ESE355: VLSI System Design

Catalog Description: Introduces techniques and tools for scalable VLSI design and analysis. Emphasis is on physical design and on performance analysis. Includes extensive lab experiments and hand-on usage of CAD tools.

Course Designation: Elective for EE and CE

Text Book: Jan Rabaey, A. Chandrakasan, B. Nikolic, "Digital Integrated Circuits: A Design Perspective", Prentice Hall, 2003.

Prerequisites: ESE218
Corequisite: none

Coordinator: Alex Doboli

Goals: The course introduces techniques and tools for scalable VLSI design and analysis. The emphasis is on physical design and on performance analysis. The course includes extensive lab experiments, a mini project and hands-on usage of CAD tools.

Objectives: Upon completion of this course, students are able to develop, layout and simulate fabricatable designs of VLSI building blocks, such as registers, arithmetic units, finite state machines, and medium-scale VLSI chips. Students are knowledgeable to design digital circuits optimized for timing and area constraints.

Topics Covered:

Week 1.	**Introduction to design of VLSI systems and circuits. The MOSFET Transistor**. Static behavior. Dynamic behavior. Secondary effects. SPICE models for the MOS transistor. Small-signal models.
Week 2.	**The CMOS Inverter**. Static behavior.
Week 3.	**The CMOS Inverter**. Dynamic behavior. Propagation delay.
Week 4.	**Combinational Logic Gates**. Complementary CMOS design
Week 5.	**Combinational Logic Gates**. Complementary CMOS design. **Layout techniques for complex gates.** Bit-slice design. Pipelining.
Week 6.	**Combinational Logic Gates**. Ratio-ed logic. Pass-transistor Logic.
Week 7.	**Combinational Logic Gates**. Dynamic CMOS. Principles. Performance. Cascading.
Week 8.	**Design of Sequential Circuits.** flip-flops. master-slave ff. CMOS static flip-flops. Implementation with PLA structures. Application.
Week 9.	**Design of Sequential Circuits.** flip-flops. master-slave ff. CMOS static flip-flops. Implementation with PLA structures. Application.
Week 10.	**Design of Sequential Circuits.** Dynamic sequential circuits. Pseudo static latch. Dynamic two-phase flip flop. C2MOS latch. NORA-CMOS structure.
Week 11.	**Design for Testability.**
Week 12.	**Interconnect.** Crosstalk. Resistive parasitic. Inductive parasitic. Packaging technology.

Week 13.	**Timing Issues in Digital Circuits.** Clock Skew. Single & two-phase clocking. countering of clock skew problems.

Class/laboratory Schedule: 3 lecture hours and 3 laboratory hours per week.

Grade = 20% Homeworks + 25% Midterm + 35% Final + 20% Project

Program Outcomes and Assessment

On the following " a-k" list, please check those topics which are covered within the course:	**% contribution***
X❑ (a) ability to apply knowledge of math, engineering, and science	
(a1) knowledge of probability and statistics, including applications to EE/CE	0%
(a2) knowledge of mathematics and of basic engineering sciences necessary to carry out analysis and design appropriate to EE/CE.	5%
(a3) knowledge of discrete mathematics or advanced mathematics (linear algebra)	0%
X❑ (b1) ability to design and conduct experiments	25%
X❑ (b2) ability to analyze and interpret data	10%
X❑ (c) ability to design system, component or process to meet needs	25%
❑ (d) ability to function on multi-disciplinary teams	
X❑ (e) ability to identify, formulate, and solve engineering problems	10%
X❑ (f) understanding of professional and ethical responsibility	5%
X❑ (g) ability to communicate effectively	10%
❑ (h) broad education	
❑ (i) recognition of need an ability to engage in life-long learning	
❑ (j) knowledge of contemporary issues	
X❑ (k) ability to use techniques, skills, and tools in engineering practice	10%
❑ Any other outcomes and assessments?	

* Assume that the total contribution of any course will be 100%. Use the right hand column to indicate the approximate percent that the left hand columns contribute to the overall course.

Americans with Disabilities Act: If you have a physical, psychological, medical or learning disability that may impact your course work, please contact Disability Support Services, ECC(Educational Communications Center) Building, Room 128, (631)632-6748. They will determine with you what accommodations, if any, are necessary and appropriate. All information and documentation is confidential.http://studentaffairs.stonybrook.edu/dss/index.shtml.

Academic Integrity: Each student must pursue his or her academic goals honestly and be personally accountable for all submitted work. Representing another person's work as your own is always wrong. Faculty is required to report any suspected instances of academic dishonesty to the Academic Judiciary. Faculty in the Health Sciences Center (School of Health Technology Management, Nursing, Social

Welfare, Dental Medicine) and School of Medicine are required to follow their school-specific procedures. For more comprehensive information on academic integrity, including categories of academic dishonesty please refer to the academic judiciary website at http://www.stonybrook.edu/commcms/academic_integrity/index.html

Critical Incident Management: Stony Brook University expects students to respect the rights, privileges, and property of other people. Faculty are required to report to the Office of University Community Standards any disruptive behavior that interrupts their ability to teach, compromises the safety of the learning environment, or inhibits students' ability to learn. Faculty in the HSC Schools and the School of Medicine are required to follow their school-specific procedures. Further information about most academic matters can be found in the Undergraduate Bulletin, the Undergraduate Class Schedule, and the Faculty-Employee Handbook.

Document Prepared by: Alex Doboli on 8/19/17