Stony Brook University

Syllabus

1. Course Staff and Office Hours

Instructor: Peter Milder
(he/him)
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Office Hours: Mondays, 1:30 to 3:30pm
Thursdays, 10:00am to 12:00pm
Light Engineering 231

Office hours may change. Please check Brightspace for up-to-date information.

2. Introduction

The field of digital system design has entered a new and complicated era. Digital designers now have increasingly large amounts of chip area to exploit, but they are strictly limited by the amount of power that can be consumed per transistor (the so-called "power wall"). Modern design practices must carefully balance a variety of system tradeoffs such as power, energy, area, throughput, latency, bandwidth, and reusability/customization of digital systems. This course will cover digital system design at the register-transfer level in SystemVerilog and study modern design abstractions, languages, and tools.

3. Course Description

Content of the course will fall into roughly three categories:

1. **Hardware Design Abstractions, Languages, and Tools:** register-transfer level design, simulation, and verification with the SystemVerilog hardware description language; parameterized "chip generator" tools; high-level synthesis (compilation of hardware from a high-level language); design-space exploration; domain-specific languages and tools.

2. **Limitations and Constraints of Modern Digital Systems:** the driving forces and limiting factors in current and near-future digital systems (the "power wall" and "utilization wall"); how these factors affect design practices and lead to a higher level of application-specific customization.

3. **New Architectures and Paradigms:** the evolution of field-programmable gate arrays; hardware architectures for deep learning applications

4. Course Catalog Description

This course focuses on languages, tools, and abstractions for design and implementation of digital systems. Course material is divided roughly into three categories: Limitations and constraints on modern digital systems; Hardware design abstractions, languages, and tools (including the SystemVerilog hardware description language); and new architectures and paradigms for digital design. Coursework will be primarily project based; there will also be reading and discussion of published papers in these areas. Students should have experience with hardware description languages (VHDL, Verilog, or SystemVerilog) and software (C, C++ or Java).
Fall, 3 credits, grading ABCF.

5. Readings

Readings for this course will be in the form of research papers, which will be distributed in class or online.

Optional reference: "SystemVerilog for Design: A Guide to Using SystemVerilog for Hardware Design and Modeling," Stuart Sutherland, Simon Davidmann, and Peter Flake. Springer.

6. Grading

Grades will be based on attendance and participation, assignments, a final examination, and a large project.

Assignments and participation	15%
Final examination	30%
Project	55%

7. Academic Honesty

Academic honesty is very important. Only put your name on your own work. Written assignments must be completed in your own words; you may not copy from other sources or use generative AI tools. For example, if you are assigned to read a research paper and answer questions about it, you may not copy text from that paper.

The use of generative AI tools (such as ChatGPT or GitHub Copilot) is prohibited in this class in all forms.

For projects, you may not share code, report, or other work outside of your group. You may not view or copy code from your classmates or show your code to them. Any copying or sharing of any work or code will result in the assignment being scored a zero for all parties involved, with no exceptions. You may not refer to code or other work from students in prior semesters or other sources online including AI generated code. For group projects, if any

member of the group commits academic dishonesty, the entire group will be equally penalized. All code will be analyzed by a plagiarism detection tool.

For the final examination, any academic dishonesty will result in failing the course.

8. Piazza: Online Discussion Forum

This course will use Piazza for class discussion. Rather than emailing questions to the teaching staff, I encourage you to post your questions on Piazza and to help answer your classmates' questions when possible. After the first day of class, you will receive an invitation sent to your stonybrook.edu email address.

9. Schedule

Classes will be held in person from 4:00pm to 5:20pm on Mondays and Wednesdays in Frey Hall 211.

The final examination will be held on Tuesday December 12 from 8:30pm to 11:00pm.

A full schedule with topics, assignments, and due dates will be available on Brightspace.

10. Student Learning Objectives

Students will acquire:

1. an ability to apply knowledge of mathematics, science, and engineering;
2. an ability to identify, formulate, and solve engineering problems;
3. an ability to communicate effectively; and
4. an ability to understand current research issues.

11. Electronic Communication Statement

Official course communication will be made by email, and by email sent via Brightspace. It is your responsibility to make sure that you read your email in your official University email account.

This course will also make use of the Piazza discussion forum, which will include announcements and clarifications. You are responsible for activating your Piazza account. Once active, Piazza messages will be sent to your official stonybrook.edu email account.

12. Student Accessibility Support Center Statement

If you have a physical, psychological, medical, or learning disability that may impact your course work, please contact the Student Accessibility Support Center, Stony Brook Union Suite 107, (631) 632-6748, or at sasc@stonybrook.edu. They will determine with you what accommodations are necessary and appropriate. All information and documentation is confidential.

Students who require assistance during emergency evacuation are encouraged to discuss their needs with their professors and the Student Accessibility Support Center. For procedures and information go to the following website: https://ehs.stonybrook.edu//programs/fire-safety/emergency-evacuation/evacuation-guide-disabilities and search Fire Safety and Evacuation and Disabilities.

13. Academic Integrity Statement

Each student must pursue their academic goals honestly and be personally accountable for all submitted work. Representing another person's work as your own is always wrong. Faculty is required to report any suspected instances of academic dishonesty to the Academic Judiciary. Faculty in the Health Sciences Center (School of Health Technology & Management, Nursing, Social Welfare, Dental Medicine) and School of Medicine are required to follow their school-specific procedures. For more comprehensive information on academic integrity, including categories of academic dishonesty, please refer to the academic judiciary website at http://www.stonybrook.edu/commcms/academic_integrity/index.html

14. Critical Incident Management Statement

Stony Brook University expects students to respect the rights, privileges, and property of other people. Faculty are required to report to the Office of Student Conduct and Community Standards any disruptive behavior that interrupts their ability to teach, compromises the safety of the learning environment, or inhibits students' ability to learn. Faculty in the HSC Schools and the School of Medicine are required to follow their school-specific procedures. Further information about most academic matters can be found in the Undergraduate Bulletin, the Undergraduate Class Schedule, and the Faculty-Employee Handbook.